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(71)Applicant : SANYO ELECTRIC CO LTD

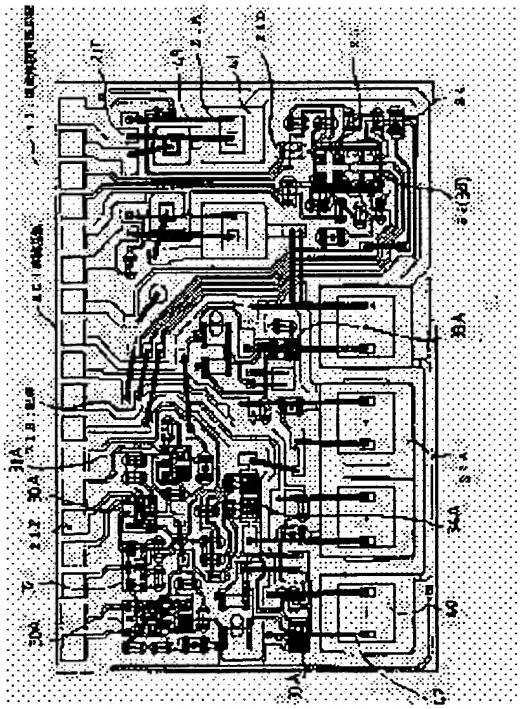
(72)Inventor : SAKAMOTO NORIAKI
KOBAYASHI YOSHIYUKI
MAEHARA EIJU
SAKAI NORIHIRO
TAKAGISHI HITOSHI
TAKAHASHI YUKITSUGU
KUSANO KAZUHISA

(54) HYBRID INTEGRATED-CIRCUIT DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To solve the problem of the conventional devices that, in a hybrid integrated-circuit device in which circuit devices are mounted on a printed circuit board, a ceramic board, a flexible sheet or the like, many circuit elements are fixed and bonded to the board, and that semiconductor elements on the circuit elements are wire-bonded by using a plurality of kinds of metal thin wires.

SOLUTION: For example, the semiconductor elements which are used for a circuit of a small signal system and Au wires which connect the semiconductor elements are formed in one package, and semiconductor devices 30A, 31A, 32, 33A, 34A, 38 are formed. Consequently, Au wire bonding operation can be omitted. When small-diameter Al wires and large-diameter Al wires are wire-bonded, the connection of the metal thin wires is completed. In the semiconductor devices, since a plurality of circuit elements are



formed on one package, the number of times of fixing and bonding operations to the mounting boards can be reduced.

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NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] About hybrid integrated circuit equipment, this invention reduces the bonding by the metal thin line, and relates to the hybrid integrated circuit equipment which can decrease in number the number of erectors.
[0002]
[Description of the Prior Art] Conventionally, an electric conduction pattern is formed on a printed circuit board, a ceramic substrate, or a metal substrate, on this, passive elements, such as active elements, such as LSI or discrete TR, a chip capacitor, a chip resistor, or a coil, are mounted, and the hybrid integrated circuit equipment set to electronic equipment is constituted. And said electric conduction pattern and said component are connected electrically, and the circuit of a predetermined function is realized.
[0003] Drawing 19 was shown as an example of a circuit. This circuit is an audio circuit and the component shown in these is mounted like drawing 20 .
[0004] In drawing 20 , an outside rectangle line is the mounting substrate 1 with which insulating processing of the front face was carried out at least most. And on this, the electric conduction pattern 2 which consists of Cu is stuck. This electric conduction pattern 2 consists of electrode 4 grades which fix electrode 2for external ejection A, wiring 2B, die pad 2C, bonding pad 2D, and a passive element 3.
[0005] In die pad 2C, TR, diode, a compound device, or LSI has fixed through solder by the shape of a bare chip. And said bonding pad 2D is electrically connected with the electrode on this chip that fixed through the metal thin lines 5A, 5B, and 5C. Generally this metal thin line is classified into a small signal and the Taishin numbers, and, as for the small signal section, the metal thin line of 20-80 micrometerphi is used. And Au line 5A or aluminum line which consists of about 40micrometerphi here is adopted. Moreover, as for the Taishin ** section, Au line or aluminum line of about 100-300 micrometerphi is adopted. Since especially the Taishin number has the large wire size, the point of cost is taken into consideration and aluminum line 5C of aluminum line 5B of 150 micrometerphi and 300 micrometerphi is chosen.
[0006] Moreover, the power TR6 which passes a high current has fixed to the heat sink 7 on die pad 2C, in order to prevent the temperature rise of a chip.
[0007] And in order to make said electrode 2for external ejection A, die pad 2C, bonding pad 2D, and an electrode 4 into a circuit, wiring 2B extends in various places. Moreover, when wiring crosses on account of the location of a chip, and the method of extension wiring, the jumping lines 8A and 8B are adopted.
[0008]
[Problem(s) to be Solved by the Invention] Many a chip capacitor, a chip resistor, TR chip for small signals, TR chips for the Taishin numbers, diodes, LSI, etc. were adopted, and each has fixed by low material etc. so that clearly also from drawing 20 . And semiconductor devices, such as TR chip, are electrically connected using the metal thin line. This metal thin line is divided into two or more kinds by

current capacity, and there are dramatically many those metal thin lines. Fixing of a chip and connection of a metal thin line lengthened like the assembler dramatically clearly like also from this thing, and lifting of cost was caused.
[0009] Moreover, recently, 0.45x0.5mm thickness has the size of a chip dramatically as small as 0.25mm, and what has a cheap unit price has come to be sold. However, when it was going to fix this chip with solder, a cone riser and since it short-circuited, the problem which is not employable as a hybrid integrated circuit substrate also had solder in the side face of a chip.
[0010] Moreover, when the package which fixed the semiconductor device to the leadframe was mounted in the hybrid integrated circuit substrate, since the size of this package was very large, there was also a problem to which the size of a hybrid integrated circuit substrate becomes large.
[0011] As stated above, even if it was going to adopt the hybrid integrated circuit substrate and was going to lower cost, there was a problem which causes lifting of cost from the point that a very small chip cannot be mounted, the point of becoming long like an erector, etc.
[0012]
[Means for Solving the Problem] The mounting substrate which accomplishes this invention in view of the technical problem mentioned above, and insulating processing of the front face is carried out at least, and has two or more electric conduction patterns in the 1st, In the hybrid integrated circuit equipment which has at least the semiconductor device connected to said electric conduction pattern and electric target, and the metal thin line which carries out bonding of the bonding electrode or said electric conduction pattern of said semiconductor device It solves by the semiconductor device which packed the semiconductor device by which bonding was carried out with said metal thin line and said metal thin line being mounted in said mounting substrate.
[0013] If the semiconductor device packed beforehand is prepared and this semiconductor device is mounted in a mounting substrate, like the erector of hybrid integrated circuit equipment, the count of bonding of a metal thin line can be reduced, and it can shorten like an assembler.
[0014] Two or more kinds of metal thin lines with which, as for said metal thin line, ingredients differ are used for the 2nd, and at least one kind of all metal thin lines are solved with being packed in said semiconductor device.
[0015] For example, what is necessary is to be able to lose the bonding of Au line and to perform only bonding of aluminum line like the erector of hybrid integrated circuit equipment, if the semiconductor device which adopts Au line is beforehand prepared as a semiconductor device when hybrid integrated circuit equipment is constituted by Au line and aluminum line. Therefore, the bonding for Au lines can be omitted from an assembly process, and can realize simplification like an assembler.
[0016] Two or more kinds of metal thin lines with which, as for said metal thin line, wire sizes differ are used for the 3rd, and at least one kind of all metal thin lines are solved with being packed in said semiconductor device.
[0017] For example, when having had good control of striking a ball in any direction with the metal thin line (300 micrometers and 150 micrometers), like an assembler, 150-micrometer bonding can be omitted by preparing the semiconductor device by which bonding is carried out with the 150-micrometer metal thin line.
[0018] To the 4th, said all metal thin lines are solved with being packed in said semiconductor device.
[0019] All the bondings of a metal thin line can be lost in the assembly of hybrid integrated circuit equipment.
[0020] The mounting substrate which insulating processing of the front face is carried out at least, and has two or more electric conduction patterns in the 5th, The semiconductor device of the small signal system connected to said electric conduction pattern and electric target, and the semiconductor device of the Taishin number system connected to said electric conduction pattern and electric target, Au line which carries out bonding of the bonding electrode and said electric conduction pattern of a semiconductor device of said small signal system at least, It is hybrid integrated circuit equipment which has at least aluminum line by which bonding is carried out to said electric conduction pattern, and solves by the semiconductor device which packed the semiconductor device by which bonding was carried out

by said Au line and said Au line being mounted in said mounting substrate.
[0021] The metal thin line by which bonding is carried out to said electric conduction pattern the 6th is solved by said aluminum line being adopted.
[0022] The mounting substrate which insulating processing of the front face is carried out at least, and has two or more electric conduction patterns in the 7th, The semiconductor device of the small signal system connected to said electric conduction pattern and electric target, and the semiconductor device of the Taishin number system connected to said electric conduction pattern and electric target, It is hybrid integrated circuit equipment which has at least Au line which carries out bonding of said electric conduction pattern, and aluminum line which carries out bonding of the semiconductor device and said electric conduction pattern of said Taishin number system at least. It solves by the semiconductor device which packed the semiconductor device of the Taishin number system by which bonding was carried out by said aluminum line and said aluminum line being mounted in said mounting substrate.
[0023] The metal thin line by which bonding is carried out to said electric conduction pattern the 8th is solved by said Au line being adopted.
[0024] The mounting substrate which insulating processing of the front face is carried out at least, and has two or more electric conduction patterns in the 9th, The semiconductor device of the small signal system connected to said electric conduction pattern and electric target, and the semiconductor device of the Taishin number system connected to said electric conduction pattern and electric target, The metal thin line of the minor diameter which carries out bonding of the bonding electrode and said electric conduction pattern of a semiconductor device of said small signal system at least, It is hybrid integrated circuit equipment which has at least the metal thin line of the major diameter which carries out bonding of said electric conduction pattern. To said mounting substrate It solves by the semiconductor device which packed the semiconductor device by which bonding was carried out with the metal thin line of said minor diameter and the metal thin line of said minor diameter being mounted.
[0025] The metal thin line by which bonding is carried out to said electric conduction pattern the 10th is solved by the metal thin line of said major diameter being adopted.
[0026] The mounting substrate which insulating processing of the front face is carried out at least, and has two or more electric conduction patterns in the 11th, The semiconductor device of the small signal system connected to said electric conduction pattern and electric target, and the semiconductor device of the Taishin number system connected to said electric conduction pattern and electric target, It is hybrid integrated circuit equipment which has at least the metal thin line of the minor diameter which carries out bonding of said electric conduction pattern, and the metal thin line of the major diameter which carries out bonding of the bonding electrode and said electric conduction pattern of a semiconductor device of said Taishin number system at least. It solves by the semiconductor device which packed the semiconductor device by which bonding was carried out with the metal thin line of said major diameter and the metal thin line of said major diameter being mounted in said mounting substrate.
[0027] The metal thin line by which bonding is carried out to said electric conduction pattern the 12th is solved by the metal thin line of said minor diameter being adopted.
[0028] The mounting substrate which insulating processing of the front face is carried out at least, and has two or more electric conduction patterns in the 13th, The semiconductor device of the small signal system connected to said electric conduction pattern and electric target, and the semiconductor device of the Taishin number system connected to said electric conduction pattern and electric target, Au line which carries out bonding of the bonding electrode and said electric conduction pattern of a semiconductor device of said small signal system at least, Two or more tracks which are hybrid integrated circuit equipment which has aluminum line which carries out bonding of said electric conduction pattern, and were separated electrically in the separation slot, Au line which connects the semiconductor device of the small signal system which fixed on said track, the semiconductor device of said small signal system, and said track, A semiconductor device with the insulating resin which covers this semiconductor device and Au line, and said separation slot between said tracks is filled up with, exposes the rear face of said track, and is supported to one is mounted in said mounting substrate. The field except the field where said semiconductor device was mounted is solved by connecting by the

connecting means except said Au line.

[0029] The mounting substrate which insulating processing of the front face is carried out at least, and has two or more electric conduction patterns in the 14th, The semiconductor device of the small signal system connected to said electric conduction pattern and electric target, and the semiconductor device of the Taishin number system connected to said electric conduction pattern and electric target, It is hybrid integrated circuit equipment which has at least Au line which carries out bonding of said said electric conduction pattern, and aluminum line which carries out bonding of the semiconductor device and said electric conduction pattern of the Taishin number system at least. Two or more tracks separated electrically in the separation slot, and the semiconductor device of the Taishin number system which fixed on said track, A semiconductor device with the insulating resin which covers aluminum line which connects the semiconductor device and said track of said Taishin number system, and the semiconductor device and aluminum line of this Taishin number system, and said separation slot between said tracks is filled up with, exposes the rear face of said track, and is supported to one is mounted in said mounting substrate. The field except the field where said semiconductor device was mounted is solved by connecting by the connecting means except said aluminum line.

[0030] The mounting substrate which insulating processing of the front face is carried out at least, and has two or more electric conduction patterns in the 15th, The semiconductor device of the small signal system connected to said electric conduction pattern and electric target, and the semiconductor device of the Taishin number system connected to said electric conduction pattern and electric target, The metal thin line of the minor diameter which carries out bonding of the bonding electrode and said electric conduction pattern of a semiconductor device of said small signal system at least, Two or more tracks which are hybrid integrated circuit equipment which has at least the metal thin line of the major diameter which carries out bonding of said electric conduction pattern, and were separated electrically in the separation slot, The metal thin line of a minor diameter which connects the semiconductor device of the small signal system which fixed on said track, the semiconductor device of said small signal system, and said track, A semiconductor device with the insulating resin which covers this semiconductor device and the metal thin line of a minor diameter, and said separation slot between said tracks is filled up with, exposes the rear face of said track, and is supported to one is mounted in said mounting substrate. The field except the field where said semiconductor device was mounted is solved by connecting by the connecting means except the metal thin line of said minor diameter.

[0031] The mounting substrate which insulating processing of the front face is carried out at least, and has two or more electric conduction patterns in the 16th, The semiconductor device of the small signal system connected to said electric conduction pattern and electric target, and the semiconductor device of the Taishin number system connected to said electric conduction pattern and electric target, It is hybrid integrated circuit equipment which has at least the metal thin line of the minor diameter which carries out bonding of said electric conduction pattern, and the metal thin line of the major diameter which carries out bonding of the semiconductor device and said electric conduction pattern of said Taishin number system. Two or more tracks separated electrically in the separation slot, and the semiconductor device of the Taishin number system which fixed on said track, The metal thin line of a major diameter which connects the semiconductor device and said track of said Taishin number system, A semiconductor device with the insulating resin which covers this semiconductor device and the metal thin line of a major diameter, and said separation slot between said tracks is filled up with, exposes the rear face of said track, and is supported to one is mounted in said mounting substrate. The field except the field where said semiconductor device was mounted is solved by connecting by the connecting means except the metal thin line of said major diameter.

[0032] The mounting substrate which insulating processing of the front face is carried out at least, and has two or more electric conduction patterns in the 17th, The semiconductor device of the small signal system connected to said electric conduction pattern and electric target, and the semiconductor device of the Taishin number system connected to said electric conduction pattern and electric target, The metal thin line of the minor diameter which carries out bonding of the semiconductor device and said electric conduction pattern of said small signal system, Two or more tracks which are hybrid integrated circuit

equipment which has at least the metal thin line of the major diameter which carries out bonding of the semiconductor device and said electric conduction pattern of said Taishin number system, and were separated electrically in the separation slot, The metal thin line which connects the semiconductor device which fixed on said track, and said semiconductor device and said track, A semiconductor device with the insulating resin which covers this semiconductor device and a metal thin line, and said separation slot between said tracks is filled up with, exposes the rear face of said track, and is supported to one is mounted in said mounting substrate. The metal thin line of said minor diameter and the metal thin line of a major diameter are solved by it being used into said semiconductor device and said metal thin line not being used for the field except the field where said semiconductor device was mounted.
[0033] To the 18th, the side face of said track is solved by changing with bow structure.
[0034] It solves by an electric conduction coat being prepared in the 19th on said track.
[0035] It connects with said track and electric target, the active element and/or passive element other than said semiconductor device are built in the 20th, and it solves by circuits also including said active element and/or said passive element being formed.
[0036] To the 21st, said track is solved by consisting of Cu, aluminum, a Fe-nickel alloy, the layered product of Cu-aluminum, and the layered product of aluminum-Cu-aluminum.
[0037] To the 22nd, said electric conduction coat turns by nickel, Au, Ag, or Pd, and is solved by a canopy top being formed to it.
[0038]
[Embodiment of the Invention] This invention relates to the hybrid integrated circuit equipment which can reduce the bonding of a metal thin line, and the die bonding of a semiconductor device especially about the hybrid integrated circuit equipment which can be simplified like an assembler.
[0039] Generally, an electronic circuitry is constituted by the circuit element with various hybrid integrated circuit equipments, and passive elements, such as active elements, such as TR chip, IC chip, or an LSI chip, a chip capacitor, or a chip resistor, are mounted as occasion demands. And these circuit elements are connected to the electric conduction pattern and the electric target which were formed on the mounting substrate. Moreover, in order to realize as a circuit, wiring is prepared in an electric conduction pattern, and the circuit element is electrically connected to it through low material, an electric conduction ball, a solder ball, conductive paste, or a metal thin line.
[0040] Especially as for the metal thin line, the wire size of the ingredient of a metal thin line and/or a metal thin line is properly used with the current capacity of the circuit block with which the circuit element to which a metal thin line is connected, or a metal thin line is used.
[0041] There are some which have been electrically connected as the 1st example by three kinds of aluminum lines, 40 micrometers, 150 micrometers, and 300 micrometers. A reason is that it obtains the direction of aluminum at a low price.
[0042] Moreover, there are some which have been electrically connected as the 2nd example by aluminum line (40-micrometer Au line, 150 micrometers, and 300 micrometers). A reason is that the Au line of bonding time amount is shorter, and it ends rather than aluminum line. It is because wedge bonding is generally used for aluminum line and it must continue applying a supersonic wave predetermined time. moreover -- if Au is used for the metal thin line of a major diameter -- a part with a thick wire size -- since it is high, aluminum line is adopted from the field of cost.
[0043] Moreover, semiconductor devices, such as TR, IC, and LSI, have a small bonding pad on the front face of a chip, and, generally Au line is adopted. However, since the chip itself is large, there is also much current capacity and the size of a bonding pad is also formed greatly, cost is taken into consideration and, as for a power transistor, Power MOS, IGBT, and SIT, a thyristor, etc. which pass a high current, aluminum line is adopted.
[0044] As mentioned above, the wire size of the ingredient of a metal thin line and a metal thin line is chosen by an area required for current capacity, cost, and bonding, reinforcement, or the class of semiconductor device by which bonding is carried out, and bonding is carried out.
[0045] The point of this invention is by fixing the packed semiconductor device to a mounting substrate to reduce the class of metal thin line connected on a mounting substrate.

[0046] For example, if the 1st example describes, it has the description to prepare separately the semiconductor device with which the semiconductor device first connected by 40 micrometers aluminum line and this 40-micrometer aluminum line became one package. And by mounting this semiconductor device by low material etc., connection of the metal thin line on a mounting substrate serves as only aluminum line (150 micrometers and 300 micrometers), and can omit all connection of 40-micrometer aluminum line.
[0047] Depending on the assembly approach, bonding equipment may change with three kinds of wire sizes, respectively. In this case, the assembly of hybrid integrated circuit equipment has the merit which all of the process which lays a mounting substrate to the bonding equipment for 40micrometer, and the process which carries out bonding can omit. The activity which lays a mounting substrate especially to bonding equipment will require a baton, and will lengthen like an assembler very well.
[0048] Moreover, the point is in the 2nd example to prepare separately the semiconductor device with which the semiconductor device connected by 40 micrometers Au line and this 40-micrometer Au line became one package. And by mounting this semiconductor device by low material etc., connection of Au line can be omitted on a mounting substrate, and the bonding process of aluminum line (150 micrometers and 300 micrometers) remains.
[0049] As for the bonding approach of Au line, unlike the bonding approach of aluminum line, bonding equipment also differs. Therefore, if connection of Au line packs all required parts, the bonding of Au line will become completely unnecessary like the assembler of hybrid integrated circuit equipment. Therefore, only the bonding of aluminum line is needed and hybrid integrated circuit equipment has the merit which can decrease the number of erectors.
[0050] Moreover, although it becomes a special example, if all metal thin lines are packed together with a semiconductor device, it sets like the assembler of hybrid integrated circuit equipment, and it is only the process which mounts a semiconductor device and all the bondings of a metal thin line can be omitted.
[0051] Since various combination can be considered and it has effectiveness in each, this invention is explained briefly [below].
[0052] The 1st combination: When the metal thin line with which wire sizes differ is adopted as a mounting substrate by N class.
[0053] Connection of the metal thin line on a mounting substrate ends by connection of the metal thin line of a class (N-1) by packing the semiconductor device by which this metal thin line was connected with at least one kind of metal thin line. As shown in drawing 1 , at least one semiconductor device is packed by one package. Moreover, a passive element or IC chip is mounted and it is good also as a hybrid mold.
[0054] The 2nd combination: When the ingredient of a metal thin line is adopted as a mounting substrate by N class.
[0055] Connection of the metal thin line on a mounting substrate ends by connection of the metal thin line of a class (N-1) by packing the semiconductor device by which this metal thin line was connected with at least one kind of metal thin line. As shown in drawing 1 , the package which adopted Au line is prepared and only bonding of aluminum line is performed in a mounting substrate side. This may prepare the package which adopted aluminum line and may perform only bonding of Au line by the mounting substrate side.
[0056] The 3rd combination: For those with N class, and the metal thin line of each ingredient, the ingredient of a metal thin line is the case where two or more wire sizes are adopted.
[0057] An easy combination explains. Ingredient aluminum 300 micrometers of wire sizes, 200 micrometers, 150 micrometers Ingredient Au It will become four kinds if an ingredient and a wire size are combined in this case 40 micrometers of wire sizes. Therefore, what is necessary will be just to adopt three or less kinds of metal thin lines at a mounting substrate side by forming the package mentioned above in at least one kind of metal thin line among four kinds of this metal thin line.
[0058] Moreover, the conveyance loss of the die bonder of the component arranged on a mounting substrate can reduce substantially. In the conventional mounting substrate like drawing 20 , installation

is needed for various locations and a component must be moved to a position. However, if the semiconductor device of this invention is adopted, since two or more kinds of semiconductor devices are packed by one, two or more components will be conveyed at once. With reference to drawing 1 , the hybrid integrated circuit equipment which adopted 40 micrometers Au line, 150 micrometers aluminum line, and 300-micrometer aluminum line is explained.

[0059] This hybrid integrated circuit equipment 13 consists of metal thin lines 42 and 43 for connecting as the electric conduction pattern 21 laid in the mounting substrate 10, the bare chips 40 and 41 which fix on this, passive elements 23 and 24, the packed semiconductor devices 30A, 31A, 32, 33A, 34A, and 38, and a circuit at least.

[0060] The electric conduction pattern 21 consists of external connection electrode 21F of business, such as electrode 21E which fixes die pad 21A, wiring 21B, bonding pad 21C, electrode 21D for passive elements, and semiconductor devices 30A, 31A, 32, 33A, 34A, and 38, wiring 21B (shown in drawing 2 convenience [of a drawing] up) of this and one, and an external lead. Moreover, a bare chip 40 is the power transistor of a BIP mold, and a bare chip 41 is Power MOS. A passive element 23 is a chip resistor and a passive element 24 is a chip capacitor. Furthermore, the metal thin line 42 is an aluminum line of a major diameter (300 micrometers), and the metal thin line 43 is an aluminum line of a minor diameter (150 micrometers).

[0061] The description of this invention is in said semiconductor devices 30A, 31A, 32, 33A, 34A, and 38. This semiconductor device surrounds an appearance by the thick wire, and is shown. Here, the circuit shown in drawing 19 was adopted as an example, and the circuit of a small signal system is packed on a scale of being various. That is, a minor diameter is sufficient as the metal thin line used for a small signal system, all of 1 ********** of the metal thin lines and semiconductor devices of this minor diameter are carried out, and it is mounted as a semiconductor device. The assembly operation on a mounting substrate stops therefore, needing the bonding of a minor diameter at all by mounting a semiconductor device. Moreover, since two or more semiconductor devices are packed, it has the description which can also reduce the number of die bondings substantially. Moreover, a passive element can also be mounted in a semiconductor device. When it considers as one package also including a passive element temporarily, the count of mounting of a passive element can also be reduced.

[0062] Moreover, it sets like an assembler, the bonding equipment of Au becomes unnecessary, and a baton becomes comparatively unnecessary [mounting to the bonding equipment of this mounting substrate]. Then, the semiconductor device packed one time is explained with reference to drawing 2 - drawing 19 . Here, the semiconductor device 38 laid in the lower right of drawing 1 is taken up and explained.

[0063] In addition, drawing 2 is the top view of a semiconductor device 38, and drawing 3 explains three types about the mounting structure of this thin semiconductor device 38. Furthermore, drawing 4 - drawing 9 R> 9 explain the manufacture approach of this semiconductor device, drawing 10 - drawing 18 explain the semiconductor device formed based on the right-hand side circuit, and drawing 19 explains the circuit constituted by the mounting substrate 10.

In the explanatory view 9 of a semiconductor device, the semiconductor device shown with the sign 53 is a semiconductor device adopted by this invention. The concrete structure of 1st semiconductor device 53A is explained first, referring to drawing 9 A. It has the tracks 51A-51C embedded to insulating resin 50, and semiconductor chip 52A fixes on said track 51A, and passive element 52B fixes this semiconductor device 53A on track 51B and 51C depending on the need. And in support of Tracks 51A-51C, it consists of said insulating resin 50.

[0064] This structure consists of three ingredients of the insulating resin 50 which embeds circuit element 52B which consists of semiconductor chip 52A, a passive element, and/or an active element, two or more tracks 51A, 51B, and 51C, and these tracks 51A, 51B, and 51C, and the separation slot 54 filled up with this insulating resin 50 is formed between tracks 51. And said tracks 51A-51C are supported with insulating resin 50.

[0065] As insulating resin, thermoplastics, such as thermosetting resin, such as an epoxy resin,

polyimide resin, and polyphenylene sulfide, can be used. Moreover, all resin can be used for it if insulating resin is resin which it can cover by carrying out the resin hardened using metal mold, DIP, and spreading. Moreover, the electric conduction foil which consists of alloys, such as an electric conduction foil which made Cu the charge of a principal member, an electric conduction foil which made aluminum the charge of a principal member, or Fe-nickel, as a track 51, the laminate of aluminum-Cu, or the laminate of aluminum-Cu-aluminum can be used. aluminum-Cu-aluminum is [as opposed to / especially / curvature] strong structure. Of course, other electrical conducting materials are possible and the electric conduction material which can be etched especially, the electric conduction material which evaporates by laser, or the comparatively soft matter which can form the separation slot 54 with a press is desirable.

[0066] Moreover, the connecting means of semiconductor device 52A and circuit element 52B is conductive paste 55C, such as low material 55B, such as metal thin line 55A, an electric conduction ball which consists of low material, an electric conduction ball which carries out flat, and solder, and Ag paste, an electric conduction coat, or anisotropy conductive resin. These connecting means are chosen with the class of a semiconductor device or circuit element 52, and a mounting gestalt. For example, if it is the semiconductor chip of raise in basic wages, as for the connection between a surface electrode and track 51B, metal thin line 55A will be chosen, and if it is CSP and SMD, a solder ball and a solder bump will be chosen. Moreover, as for a chip resistor and a chip capacitor, solder 55B is chosen. Since there is no elutriation from the chip of a metal thin line when mounted by face down, the package near a real chip size is attained.

[0067] Moreover, as for fixing with semiconductor device 52A and track 51A, an electric conduction coat is adopted. This electric conduction coat should just exist further at least here.

[0068] The ingredient considered as this electric conduction coat is Ag, Au, Pt, Pd, or low material, and is covered with covering under low vacuums, such as vacuum evaporationo, sputtering, and CVD, or a high vacuum, plating, sintering, or spreading.

[0069] For example, Ag pastes up with Au and pastes up low material. Therefore, if Au coat is covered by the chip rear face, by covering Ag coat, Au coat, and a solder coat to track 51A as it is, the thermocompression bonding of the semiconductor chip can be carried out, and a chip can be fixed through low material, such as solder. Here, said electric conduction coat may be formed in the maximum upper layer of the electric conduction coat by which the laminating was carried out to two or more layers. For example, on track 51A of Cu, that with which the bilayer of the thing and Ag coat on which three layers of the thing and nickel coat on which the bilayer of nickel coat and Au coat was put in order, Cu coat, and a solder coat were put in order, and nickel coat was covered in order can be formed. In addition, although a large number [the class of these electric conduction coat, and a laminated structure] besides this, they omit here.

[0070] Since this semiconductor device 53A is supporting the track 51 by the insulating resin 50 which is closure resin, the support substrate which carries out lamination support of the track becomes unnecessary, and it consists of a track 51, a component 52, and insulating resin 50. This configuration is the description of this invention. Since the track of the conventional circuit apparatus is supported and stuck with a support substrate (a printed circuit board, a ceramic substrate, or flexible sheet) or is supported by the leadframe, the configuration which is originally needlessness is added. However, this semiconductor device consists of necessary minimum elements, can do a support substrate as it is unnecessary, and it has the part and the description it is featureless to it being cheap with a thin shape.

[0071] Moreover, it has insulating resin 50 which the circuit element 52 other than said configuration is covered, and said separation slot 54 between said tracks 51 is filled up, and is supported to one.

[0072] Between this track 51, it becomes the separation slot 54, and it is filling up with insulating resin 50 here, and has the merit which can aim at each other insulation.

[0073] Moreover, it has insulating resin 50 which covers a component 52, and the separation slot 54 between tracks 51 is filled up with, exposes the rear face of a track 51, and is supported to one.

[0074] The point of exposing the rear face of this track is one of the descriptions of this invention. The rear face of a track can present connection with the exterior, and has the description which can make

unnecessary the through hole adopted in the printed circuit board which adopted the support substrate.
[0075] And when semiconductor device 52A has fixed directly through electric conduction coats, such as low material, and Au, Ag, the rear face of a track 51 can be exposed, it can accumulate, and the heat generated from semiconductor device 52A can be told to a mounting substrate through track 51A. It is effective in the semiconductor chip whose property improvement of lifting of an actuation current etc. is attained especially by heat dissipation. This is the point of this semiconductor device 53A, and mentions later about this.
[0076] Moreover, this semiconductor device 53A has structure which is carrying out real coincidence in the rear face of the separation slot 54 and a track 51. This structure is the description of this invention, and since a level difference is not prepared in the rear face of a track 51, it has the description which can move a semiconductor device 53 horizontally as it is.
[0077] Moreover, this invention has applied the insulating coats RF, such as a solder resist, in order to realize a mounting substrate and multilayer structure. And wiring of the mounting substrate 10 is made to extend at the rear face of semiconductor device 53A by exposing a part of track 51. A track 51 and metal thin line 55A work as a conventional jumping wire, and realize multilayer structure because this semiconductor device fixes to the mounting substrate 10. About this, it mentions later.
[0078] Furthermore, the semiconductor device and/or passive element of a small signal system as which the metal thin line of a minor diameter is adopted are taken up, and this invention is packed, as shown in drawing 10 - drawing 18 . Since it is a small signal system, as for a metal thin line, aluminum or Au of a minor diameter is adopted. In addition, Au line of 40 is adopted here.
[0079] Then, the reason of adoption of this Au line is explained.
[0080] As for the reason, the mould of the insulating resin is carried out by the transfer mold, and the deformation resistance over transfer pressure is because the direction of Au is excellent. It connects by wedge bonding, and it is weak, and a bonding field is larger than Au, and the part of a neck is required for aluminum line, and it has the fault to which the size of a semiconductor device becomes large. Furthermore, aluminum line has the fault it is decided to the wedge-bonding section that the direction of a drawer will be so that it may turn out that drawing 1 and drawing 20 are seen. Since it is ball bonding, it can do the direction of a drawer of a line freely, and Au line has a quick bonding speed, and a limit is not added to the location of the track by which bonding is carried out by the part and aluminum bonder, but it has rather than them the merit which can be arranged freely. Therefore, the location of the track used as a bonding pad can be arranged to a free area, and the shrink of the part semiconductor device becomes possible.
Unlike semiconductor device 51A which the rear-face structure of a track 51 shows to drawing 9 A, semiconductor device 53B shown in explanatory view 9 of semiconductor device 53B B is real identitas except it. Here, this different part is explained.
[0081] As shown also in drawing, the rear face of a track 51 is dented rather than the rear face (rear face of the insulating resin 50 with which the separation slot 54 was filled up) of insulating resin 50. By making it this structure, a multilayer interconnection becomes possible. For details, it mentions later.
Unlike the semiconductor devices 51A and 51B which the rear-face structure of a track 51 shows to drawing 9 A and drawing 9 B, semiconductor device 53C shown in explanatory view 9 C of semiconductor device 53C is real identitas except it. Here, this different part is explained.
[0082] As shown also in drawing, the rear face of a track 51 projects rather than the rear face (rear face of the insulating resin 50 with which the separation slot 54 was filled up) of insulating resin 50. By making it this structure, a multilayer interconnection becomes possible. For details, it mentions later.
explanation of the manufacture approach of semiconductor devices 53A-53C -- the manufacture approach of a semiconductor device 53 is explained using drawing 4 - drawing 9 below.
[0083] The sheet-like electric conduction foil 60 is first prepared like drawing 4 . As for this electric conduction foil 60, the electric conduction foil which the adhesion of low material, bonding nature, and plating nature are taken into consideration, and that ingredient is chosen, and consists of the electric conduction foil which made Cu the charge of a principal member as an ingredient, the electric conduction foil which made aluminum the charge of a principal member, or the alloy of Fe-nickel, the

layered product of aluminum-Cu, the layered product of aluminum-Cu-aluminum, etc. are adopted.
[0084] When the thickness of an electric conduction foil took next etching into consideration, 35 micrometers - about 300 micrometers were desirable, and 70 micrometers (2 unciae) copper foil was adopted here. However, 300 micrometers or more or at least 10 micrometers or less are fundamentally good. What is necessary is just to be able to form the separation slot 61 shallower than the thickness of the electric conduction foil 60 so that it may mention later.
[0085] In addition, by predetermined width of face, it is wound in the shape of a roll, and is prepared, and it may be conveyed by each process which this mentions later, the electric conduction foil cut into predetermined magnitude may be prepared, and the sheet-like electric conduction foil 60 may be conveyed by each process mentioned later. Then, there is a process which removes more thinly than the thickness of the electric conduction foil 60 the electric conduction foil 60 except the field which serves as a track 51 at least (see drawing 4 above).
[0086] First, Photoresist (etching-proof mask) PR is formed on the Cu foil 60, and patterning of the photoresist PR is carried out so that the electric conduction foil 60 except the field used as a track 51 may be exposed (see drawing 5 above). And what is necessary is just to etch through said photoresist PR (see drawing 6 above).
[0087] The depth of the separation slot 61 formed of etching is 50 micrometers, and since the side face turns into a split face, its adhesive property with insulating resin 50 improves.
[0088] Moreover, the side attachment wall of this separation slot 61 serves as structure which changes with clearance approaches. Evaporation by wet etching, dry etching, and laser and dicing can be used for this clearance process. Moreover, you may form with a press. In the case of wet etching, as for etchant, a ferric chloride or a cupric chloride is mainly adopted, dipping of said electric conduction foil is carried out into this etchant, or a shower ring is carried out by this etchant. Since wet etching is generally etched into a non-anisotropy, a side face becomes bow structure here, as shown in drawing 6 B.
[0089] Moreover, in the case of dry etching, it can etch by the anisotropy and the non-anisotropy. Although it is said in current that it is impossible to remove Cu by reactive ion etching, it is removable by sputtering. Moreover, it can etch by the anisotropy and the non-anisotropy according to the conditions of sputtering.
[0090] Moreover, by laser, a direct laser beam is applied, a separation slot can be formed, and the side face of the separation slot 61 is rather formed straight in this case.
[0091] Moreover, although it is impossible in dicing to form the bent complicated pattern, it is possible to form a grid-like separation slot.
[0092] In addition, in drawing 6 , a corrosive resistant electric conduction coat may be selectively covered to an etching reagent instead of Photoresist PR. If a track and the part which changes are covered selectively, this electric conduction coat turns into an etching protective coat, and a separation slot can be etched, without adopting a resist. The ingredient considered as this electric conduction coat is nickel, Ag, Au, Pt, or Pd. And the electric conduction coat of these corrosion resistance has the description utilizable as it is as a die pad and a bonding pad.
[0093] For example, it pastes up with Au and low material pastes up Ag coat. Therefore, if Au coat is covered by the chip rear face, the thermocompression bonding of the chip can be carried out to Ag coat on a track 51 as it is, and a chip can be fixed through low material, such as solder. Moreover, since Au thin line can be pasted up on the electric conduction coat of Ag, wire bonding also becomes possible. Therefore, it has the merit which can utilize these electric conduction coats as a die pad and a bonding pad as they are. see drawing 6 above)
Then, there is a process which connects with the electric conduction foil 60 with which the separation slot 61 was formed electrically, and mounts a circuit element 52 in it like drawing 7 .
[0094] As a circuit element 52, they are passive element 52B, such as semiconductor device 52A, such as a transistor, diode, and IC chip, a chip capacitor, and a chip resistor. Moreover, although thickness becomes thick, the semiconductor device of face down molds, such as CSP, BGA, and SMD, can also be mounted.
[0095] Here, as a semiconductor chip of raise in basic wages, die bonding of the transistor chip 52A is

carried out to track 51A, and an emitter electrode, track 51B and a base electrode, and track 51B are connected by the ball bonding by thermocompression bonding using Au line 55A.
[0096] In addition, aluminum line which fixed by the wedge bonding by the supersonic wave etc. may be adopted. Moreover, 52B is a passive element and/or active elements, such as a chip capacitor, and a chip capacitor is used for it here and it fixes by low material, such as solder, or conductive paste 55B. see drawing 7 above)
Furthermore, as shown in drawing 8 , there is a process which adheres insulating resin 50 to said electric conduction foil 60 and the separation slot 61. This is realizable with a transfer mold, injection molding, or dipping. As a resin ingredient, thermosetting resin, such as an epoxy resin, can be realized by the transfer mold, and thermoplastics, such as polyimide resin and polyphenylene sulfide, can be realized by injection molding.
[0097] the thickness of the insulating resin covered with the gestalt of this operation by electric conduction foil 60 front face -- about [from the maximum crowning of a circuit element] -- it is adjusted so that about 100 micrometers may be covered. This thickness can also be made [also thickening in consideration of reinforcement, and] thin.
[0098] The description of this process is that the electric conduction foil 60 used as a track 51 serves as a support substrate until it covers insulating resin 50. For example, although the support substrate (a printed circuit board and flexible sheet) which originally is not needed is adopted and the track is formed in CSP which adopted the printed circuit board and the flexible sheet, the electric conduction foil 60 used as a support substrate is an ingredient required as a track in this invention. Therefore, it has the merit which can work excluding a component as much as possible, and lowering of cost can also be realized. Moreover, since the place of a dicing line does not have an electric conduction foil, the blinding of a blade can be prevented. Furthermore, when the mould of the package which adopted the ceramic substrate is carried out and it carries out dicing, destruction of a blade and wear are intense, but in this invention, in order to carry out the dicing only of the resin, it has the merit which can lengthen the life of a blade.
[0099] Moreover, since the separation slot 61 is formed more shallowly than the thickness of an electric conduction foil, the electric conduction foil 60 is not separately separated as a track 51. Therefore, in case it can be dealt with from mounting of a circuit element to dicing and the mould especially of the insulating resin is carried out by one as a sheet-like electric conduction foil 60, it has the description to which conveyance to metal mold and the activity of mounting to metal mold become very easy. see drawing 8)
Then, there is a process separated as a track 51, removing the rear face of the electric conduction foil 60 chemically and/or physically. This process to remove is given by polish, grinding, etching, metal evaporation of laser, etc. here.
[0100] In the experiment, about 30 micrometers of whole surface are deleted with polish equipment or grinding attachment, and insulating resin 50 is exposed from the separation slot 61. By drawing 8 , a dotted line shows this field exposed. Moreover, in order to make wiring on a mounting substrate extend, it is drawing 9 A which forms the insulating coat RF in the rear face of semiconductor device 53A. Consequently, it dissociates as a track 51 with a thickness of about 40 micrometers.
[0101] Moreover, like drawing 9 B, insulating resin 50 is exposed, and in order to adopt the structure of denting the rear face of a track 51 rather than the rear face of insulating resin 50, overall etching of the electric conduction foil 60 may be carried out.
[0102] Furthermore, like drawing 9 C, an etching-proof mask may be formed in the rear face of a track, and may be etched so that a part of track may be exposed. In this case, a track 51 projects rather than the rear face of insulating resin 50.
[0103] Whichever it is structure, it becomes the structure which the rear face of a track 51 exposes from insulating resin 50. And the separation slot 61 is deleted and it becomes the separation slot 54. (Refer to drawing 9 above) Finally electric conduction material, such as solder, is put on the track 51 exposed as occasion demands, the multilayer structure of a mounting substrate is further taken into consideration, insulating resin is covered with the need by the rear face of a semiconductor device 53, and it completes

as a semiconductor device.
[0104] In addition, when putting an electric conduction coat on the rear face of a track 51, an electric conduction coat may be beforehand formed in the rear face of the electric conduction foil of drawing 4 . In this case, what is necessary is just to put the part corresponding to a track selectively. The covering approach is plating. Moreover, this electric conduction coat has the good ingredient which is tolerant to etching. Moreover, when this electric conduction coat or photoresist is adopted, it can dissociate as a track 51 only by etching, without grinding, and structure of drawing 9 C can be realized.
[0105] In addition, by this manufacture approach, although the semiconductor chip and the chip capacitor are only mounted in the electric conduction foil 60, you may arrange in the shape of a matrix by making this into one unit.
[0106] Moreover, a transistor, diode, and one IC or LSI may be mounted as an active element (semiconductor chip), and you may form as a discrete mold. see drawing 13 - the drawing 1414) Moreover, two or more said active elements are mounted, and it is good also as a semiconductor device of a compound die. see drawing 11 , drawing 12 , and drawing 14)
Furthermore, a chip resistor and a chip capacitor may be mounted as a transistor, diode, IC or LSI, and a passive element as an active element (semiconductor chip), and you may constitute from forming wiring as a track as a hybrid IC mold. see drawing 10 , drawing 12 , drawing 16 , drawing 17 , and drawing 18)

And when it has arranged in the shape of a matrix, after a track is separated, it is separately separated by dicing equipment.
[0107] By the above manufacture approach, a track 51 is embedded to insulating resin 50, and the flat semiconductor device 53 in which the rear face of insulating resin 50 and the rear face of a track 51 carry out real coincidence can be realized.
[0108] This manufacture approach has the description which utilizes insulating resin 50 as a support substrate, and can perform the separation activity of a track 51. Insulating resin 50 is an ingredient required as an ingredient which embeds a track 51, and does not need an unnecessary support substrate. Therefore, it can manufacture with the minimum ingredient and has the description which can realize reduction of cost.
[0109] In addition, the thickness of the insulating resin formed upwards from track 51 front face can be adjusted at the time of adhesion of insulating resin. Therefore, although it changes with circuit elements mounted, the thickness as a semiconductor device 53 has the description made also thickly and thinly. Here, it becomes the semiconductor device with which the 40-micrometer track 51 and the semiconductor device were embedded to the insulating resin 50 of 400-micrometer thickness.
It explains referring to drawing 2 and drawing 3 R> 3 about the hybrid integrated circuit equipment of explanation of the mounting structure on a mounting substrate, then this invention. Drawing 2 is the top view of hybrid integrated circuit equipment, and the sectional view in the A-A line of drawing 2 is drawing 3 . In addition, the structure which fixed semiconductor device 53C of semiconductor device 53B and drawing 9 C of semiconductor device 53of drawing 9 A A and drawing 9 B to the mounting substrate 10 is shown in drawing 3 A, drawing 3 B, and drawing 3 C.
[0110] The mounting substrate 10 is explained first. As a mounting substrate 10 which mounts the semiconductor device 53 mentioned above, a printed circuit board, a ceramic substrate, a flexible sheet substrate, or a metal substrate can be considered. Since the electric conduction pattern 21 is formed in a front face, an electric insulation is taken into consideration and, as for this mounting substrate 10, insulating processing of the front face of a substrate is carried out at least. Since the substrate itself consists of insulating materials, a printed circuit board, a ceramic substrate, and a flexible sheet substrate should just form the electric conduction pattern 21 in a front face as it is. However, in the case of the metal substrate, an insulating material is put on a front face at least, and the electric conduction pattern 21 is put on this. In addition, with the gestalt of this operation, the electric conduction pattern formed in the mounting substrate 10 is used as the electric conduction pattern 21, and the electric conduction pattern supported by the insulating resin 50 of a semiconductor device 53 is distinguished as a track 51, and is explained.

[0111] Into the electric conduction pattern 21, electrode 21E (in addition, by drawing 1 , since it is hard to distinguish, shown in drawing 2 and drawing 3 .) which fixes electrode 21D which fixes die pad 21A, wiring 21B, bonding pad 21C, a chip resistor 23, and a chip capacitor 24, and this semiconductor device 53, and external connection electrode 21F which are prepared further as occasion demands are prepared so that drawing 1 may also show. In addition, in drawing 2 , the thick continuous line showed electrode 21E and wiring 21B of this and one which fix this semiconductor device 53.
[0112] On the other hand, in a semiconductor device 53, there is track 51E used as track 51A which fixed semiconductor chip 52A, a bonding pad, track 51B which changes and Tracks 51A and 51B, and wiring prepared by one in the track 51 supported by insulating resin 50.
[0113] Moreover, the part of the ellipse form of drawing 2 shows the contact section 24 electrically connected with electrode 21E on the mounting substrate 10 in the rear face of a semiconductor device 53. And according to the rear-face structure shown in this contact section 24, drawing 3 A - drawing 3 C, it became semiconductor device 53 rear face so that wiring 21B of the mounting substrate 10 could extend.
[0114] In addition, since the structure of a semiconductor device 53 is already explained, detailed explanation is omitted.
The insulating coat RF is formed in the rear face of rear-face structure book semiconductor device 53A of semiconductor device 53A shown in drawing 3 A, and said contact section 24 is exposed to it through this insulating coat RF. This semiconductor device 53 can cover a track 51 by adopting the insulating coat RF, although all tracks are originally the structures exposed from a rear face as drawing 8 R> 8 and drawing 9 also show.
[0115] Therefore, it has the description which can make wiring 21B formed in the mounting substrate 10 extend at the rear face of a semiconductor device 53.
[0116] The 1st description of this invention is closed by insulating resin 50 as a semiconductor device 53, and track 51A which semiconductor chip 52A fixed has it in fixing with the track 21 on the mounting substrate 10.
[0117] The heat generated in semiconductor chip 52A radiates heat to track 21E on the mounting substrate 10 through track 51A so that clearly also from the sectional view of drawing 3 . Since it excels in heat conduction by electric conduction material, track 21E can tell the heat of semiconductor chip 52A to the mounting substrate 10 side. Moreover, the heat which gets across to metal thin line 55A can also be told to a track through track 51B with comparatively large size of a rectangular parallelepiped. These tracks 21 become by wiring 21B and one, and heat is emitted to an external ambient atmosphere through wiring 21B. Therefore, the temperature rise of a semiconductor chip 10 can be prevented and buildup of the part which can control the temperature rise of a semiconductor chip, and an actuation current is enabled.
[0118] If especially the mounting substrate 10 consists of metal substrates, the heat of semiconductor chip 52A can be told to a metal substrate through a track 21. This metal substrate can be committed as a big heat sink and a heat sink, and can prevent the temperature rise of a semiconductor chip further rather than other mounting substrates mentioned above.
[0119] In the case of a metal substrate, the short circuit between tracks is taken into consideration, an insulating material is given to a front face, and an inorganic substance and the organic substance can be considered as an ingredient. Here, an epoxy resin, polyimide resin, etc. are adopted. Although thermal resistance can be comparatively made small since this ingredient is thinly formed with 30-300 micrometers, thermal resistance can be further made small by mixing fillers, such as a silica and an alumina, into insulating resin.
[0120] The 2nd description is in the insulating coat RF. Wiring 21B can be made to extend under semiconductor device 53A by covering the insulating coat RF so that the contact section 24 mentioned above may be exposed. Therefore, by using the track 51 of semiconductor device 53A, and metal thin line 55A, multilayer-interconnection structure can be realized and wiring on the mounting substrate 10 can be simplified. The substrate size of the hybrid IC of the former shown in drawing 20 and the hybrid IC shown in drawing 1 is the same, and it is designed. If each pattern is compared, the rough next door

and the fine pattern of spacing of a circuit pattern have decreased [the direction of the hybrid IC of this invention]. This is because it connects with the electric conduction pattern 21 on the mounting substrate 10 through opening of the insulating coat RF and the track 51 by the side of a semiconductor device 53 is covered with the insulating coat RF except it. Since this track can be formed also as wiring, the crossover of it was attained and it has realized multilayer structure together with a metal thin line. Therefore, in the process which mounts a component in a mounting substrate, if a semiconductor device is prepared beforehand, it has the description with which the count of bonding for a crossover adopted on a mounting substrate can also decrease. Furthermore, it has the description which can also reduce the complicated circuit pattern for avoiding a crossover on a mounting substrate.

[0121] Furthermore, the 3rd description is in a metal thin line, and it has the description which can reduce a bonding process. In the hybrid IC of drawing 20 , it divides into the semiconductor device handling a small signal, and the semiconductor device treating the Taishin number, and the wire size of a metal thin line is used properly. That is, the metal thin line handling a small signal for semiconductor devices was shown by the thin continuous line, and 40-micrometer Au line is used for it. And ball bonding of this Au thin line is carried out. Moreover, the metal thin line treating the Taishin number for semiconductor devices was shown by the thick wire, and 100 micrometers - 300 micrometers aluminum line is used for it. Here, 150-micrometer aluminum line is adopted as the object for the gate electrodes of Power MOS, and a jumping line, and 300-micrometer aluminum line is adopted as the source electrode of Power MOS, the base of a power transistor, an emitter electrode, and a jumping line. And SUTITCHI bond of these aluminum line is carried out. In addition, Au line may be adopted instead of aluminum line.

[0122] This invention has the description in wiring 51E which extends in the semiconductor device to which Au line was connected, the bonding pad to which Au line is connected, a bonding pad, and one, and the semiconductor device which comes to close a die pad by one by insulating resin 50.

[0123] All the semiconductor devices that adopted this metal thin line of Au become unnecessary [the bonding of Au on the mounting substrate 10] by preparing as a semiconductor device 53, and have the merit which can reduce bonding processes. Furthermore, the count of mounting of a circuit element including this semiconductor device can also be reduced substantially. Moreover, although three kinds of bonders needed to be prepared and bonding needed to be carried out by each bonder by adopting said three kinds of metal thin lines in the former, it has the merit which can omit the bonder of Au line in this invention. Therefore, simplification of a facility can also be attained, moreover, what is necessary is just to put a mounting substrate on two kinds of bonders, and it can attain simplification of a process.

[0124] Especially a semiconductor device can be further formed also as a hybrid IC also as a compound device also as a discrete device, theoretically, can incorporate all circuit elements as a semiconductor device, and can reduce substantially the number of component fixing to a mounting substrate top.

[0125] A semiconductor device with the small 0.45x0.5 thickness of 0.25mm etc. can be used for the 5th description, and the reduction of cost of it is attained.

[0126] As the conventional example also explained, even if it was going to adopt the cheap small chip of a price, at the former, the problem Fukiage carries out [the problem / solder] a ** short circuit was in the side face of a chip with 0.45x0.5mm and a small chip [like / with a thickness of 0.25mm].

[0127] However, in this invention, Au bump was put on the semiconductor chip 52A rear face, and a track 51 and semiconductor chip 52A were fixed through this bump, and after completing as a semiconductor device 53, it has fixed to the mounting substrate 10. Therefore, even if it fixed this semiconductor device 53 using solder, since the side face of semiconductor chip 52A was covered with insulating resin 50, the problem of a short circuit of it mentioned above is lost, and it could adopt the semiconductor chip with small size.

rear-face structure book semiconductor device 53of semiconductor device 53B shown in drawing 3 B B -- semiconductor device 53A and parenchyma of drawing 3 A -- it is the same and a different point is having dented the track 51 exposed to the rear face of semiconductor device 53B rather than insulating resin 50.

[0128] The description of this invention is in the depression of said track 51. for this depression, the

electric conduction pattern 21 by the side of the track 51 of semiconductor device 53B and said mounting substrate 10 has desired spacing -- things are made. Therefore, wiring 21B can be made to extend under semiconductor device 53B like semiconductor device 53A. Therefore, by using the track 51 of semiconductor device 53B, and metal thin line 55A, multilayer-interconnection structure can be realized and wiring on the mounting substrate 10 can be simplified.

[0129] In addition, the insulating coat RF may be covered at the rear face like semiconductor device 53A.

rear-face structure book semiconductor device 53C of semiconductor device 53C shown in drawing 3 C -- the semiconductor devices 53A and 53B of drawing 3 A and drawing 3 B, and parenchyma -- it is the same and a different point is a point that the track 51 exposed to the rear face of semiconductor device 53B projects rather than insulating resin 50.

[0130] The description of this invention is in projection of said track 51. This projection structure can prepare desired spacing in the electric conduction pattern 21 by the side of the track 51 of semiconductor device 53C, and said mounting substrate 10. Therefore, wiring 21B can be made to extend under semiconductor device 53C like semiconductor devices 53A and 53B. Therefore, by using the track 51 of semiconductor device 53C, and metal thin line 55A, multilayer-interconnection structure can be realized and wiring on the mounting substrate 10 can be simplified.

[0131] In addition, the insulating coat RF may be covered at the rear face like semiconductor device 53A. Then, the circuit adopted as this hybrid integrated circuit equipment and the part constituted as a semiconductor device in this circuit are explained with reference to drawing 10 R> 0 - drawing 18 , adopting drawing 19 .

[0132] Drawing 19 is an audio circuit and Audio from the left. Amp Onech circuit section, Audio Amp Twoch circuits sections and the change power circuit section are surrounded with a thick alternate long and short dash line, and it is shown.

[0133] Moreover, the circuit surrounded as the continuous line is formed in each circuit section as a semiconductor device. It is Audio first. Amp In 1ch circuit section, three kinds of semiconductor devices and two semiconductor devices which were united with 2ch circuits sections are prepared.

[0134] The current Miller circuit which changes by TR1 and TR2, and the differential circuit which consists of TR3 and TR4 are united, and 1st semiconductor device 30A is constituted, as shown in drawing 19 . This semiconductor device 30A is shown in drawing 10 . Here, four 0.55x0.55x0.24mm transistor chips are adopted, and bonding is carried out with Au thin line. In addition, the size of semiconductor device 30A is 2.9x2.9x0.5mm.

[0135] Moreover, the contact section shown by the dotted line is 0.3mmphi. The figure shown in **** is a terminal number, and B and E show the base and an emitter. Drawing 11 or subsequent ones of these notations is the same.

[0136] 2nd semiconductor device 31A constitutes a part of Puri driver line from TR6 and D2 of drawing 19 . The Puri driver line consists of TR6, D2, R3, and R8, and makes TR9 and TR10 of an output stage drive. This semiconductor device 31A is shown in drawing 11 , and two TR(s) adopt the semiconductor chip which consisted of one chips, and form diode D2 using the PN junction between base emitters. D2 is 0.75x0.75x0.145mm, TR6 is 0.55x0.55x0.24mm in chip size, and the appearance of semiconductor device 31A is 2.1x2.5x0.5mm here.

[0137] The 3rd semiconductor device 32 constitutes the differential current regulator circuit for passing the current stabilized in the differential circuit to fluctuation of supply voltage, and consists of TR5, TR15, and D1 of drawing 19 . In addition, D1 is the constant current bias diode of a differential circuit and the Puri driver line. This semiconductor device 32 is shown in drawing 12 , as for TR5 and TR15, 0.55x0.55x0.24mm and D1 are 0.75x0.75x0.145mm in size, and the appearance of a semiconductor device 32 is 2.1x3.9x0.5mm.

[0138] 4th semiconductor device 33A is the temperature compensation transistor TR8 shown in drawing 19 , and compensates an idling current to temperature fluctuation of a mounting substrate. This TR8 consists of 1 chip semiconductor devices (0.75x0.75x0.145) shown in drawing 13 . When this is formed as semiconductor device 33A, an appearance is 2.3x1.6x0.5mm.

[0139] The 5th semiconductor device 34 is [TR7 and] Audio of the PURIDO rye bar current regulator circuit which consists of TR7, R6, and R7 of drawing 19 . Amp Two chips of TR17 which constitutes the PURIDO rye bar current regulator circuit of 2ch circuits sections become one package. As this semiconductor device 34A is shown in drawing 14 , it is that from which the transistor (0.55x0.55x0.24mm) of an item became 2 reams, and an appearance is 2.3x3.4x0.5mm.
[0140] In addition, semiconductor device of 2 ream 34A may be constituted according to an individual. In this case, the semiconductor device 35 with which only one chip shown in drawing 15 was closed is adopted. The appearance of this semiconductor device 35 is 2.3x1.6x0.5mm.
[0141] Moreover, since 30B, 31B, and 33B which are shown in drawing 19 are the same circuit as 30A, 31A, and 33A, explanation is omitted.
[0142] In addition, TR9 and TR10 are output stage power transistors, and R1, C1, and C2 are the components for abnormality oscillation prevention. On the other hand, the change power circuit section shown in the right-hand side of drawing 19 The supply voltage change circuit which consists of TR41, TR51, R41, R43, R51, and R53, The comparator for a supply voltage change which consists of TR43, TR53, R40, R42, R50, and R52, It consists of diodes for rectification which consist of a RF amendment circuit which consists of diodes D45, D55, C43, and C53, and diodes D42, D43, D52, and D53.
[0143] In the power circuit of drawing 19 , as for the 6th semiconductor device 36, diodes D42 and D43 and zener diode D45 grow into one package. The semiconductor chip mounted as a semiconductor device consists of TR chips, and constitutes diodes D42 and D43 from a PN junction between base-collectors. Moreover, in drawing 16 , TR and zener diode which were surrounded by the dotted line were mounted with one chip, and D45 uses the zener diode of this component. Moreover, in order to compensate the sag by the temperature rise of zener diode, the diode between base-emitters of TR built in together is used. In addition, the appearance of 0.6x0.6x0.24 and other TR(s) of the appearance of TR with Zener is 0.35x0.35x0.24. And the appearance of the package with which these were closed is 1.9x4.4x0.5mm.
[0144] In the power circuit of drawing 19 , as for the 7th semiconductor device 37, diodes D52 and D53 and zener diode D55 grow into one package. The transistor corresponding to D53 and D52 in the semiconductor chip mounted as a semiconductor device is an PNP mold, and although structures differ a little, the mounting gestalt is the same as drawing 16 and parenchyma. As for the 8th semiconductor device 38 of drawing 18 , TR43 and TR53 grow into one package with the circuit of drawing 16 and drawing 17 . In addition, the appearance of the package with which these were closed is 4x5.7x0.5mm. And this semiconductor device 38 is mounted as a semiconductor device 53 of drawing 1 and drawing 2 . As explained above, this semiconductor device can consist of a discrete mold which mounted one TR, or a hybrid IC mold which mounted two or more TR(s) and constituted the desired circuit. Here, although constituted only from TR, two or more components also including IC, LSI, a system LSI, and a passive element may be mounted. In an experiment, although 5x5.7x0.5mm is max, the circuit element mounted may be increased and you may make it larger magnitude than this. The wiring putter is simplified so that it may understand, even if what mounted these semiconductor devices in the mounting substrate 10 is shown in drawing 1 and compares from the mounting substrate of the conventional type of drawing 20 .
[0145] Drawing 21 explains how many sizes become small by adopting the semiconductor device of this invention. The photograph shown in drawing is this scale factor, and shows the semiconductor device of the compound SMD which adopted the item SMD which adopted the leadframe from the left, and the leadframe, and also this invention. As for Item SMD, one TR is carried out, and, as for Compound TR, the mould of the two TR(s) is carried out. The circuit which shows the semiconductor device of this invention to drawing 10 is constituted, and four TR(s) are closed. In spite of closing the component of two times compound [SMD] so that clearly also from drawing, the size of this semiconductor device is only a little larger than the compound SMD also including a leadframe. In addition, the semiconductor device 35 of drawing 15 R> 5 with which one TR was closed was shown most in right-hand side. This invention can realize small and a thin semiconductor device, and it is the the best for portable electronic equipment so that it may understand from now on.

[0146]
[Effect of the Invention] in this invention, the erector of a mounting substrate can reduce a number substantially in two or more kinds of metal thin lines adopted as hybrid integrated circuit equipment by preparing beforehand at least one kind of metal thin line, and the semiconductor device which closed the semiconductor device connected to this by one so that clearly from the above explanation .
[0147] For example, with the hybrid integrated circuit equipment which adopts 40 micrometers Au line, 150 micrometers aluminum line, and 300-micrometer aluminum line, since the semiconductor device to which Au line was connected was made one package also including Au line and it has fixed to the mounting substrate, connection of the metal thin line on a mounting substrate should just carry out wire bonding only of the aluminum line. Therefore, the wire-bonding equipment for Au lines can exclude from this assembly process, and can also exclude this bonding. Moreover, the bonding of easy ******, a semiconductor device, or a passive element also becomes unnecessary about one package and the semiconductor device which changed by two or more semiconductor devices, and two or more semiconductor devices and two or more passive elements.
[0148] Therefore, it assembles, and since a process becomes short and a baton also becomes short, it has the description to which the delivery date to a user becomes short, and **** and a manufacturing cost become cheap.
[0149] Moreover, insulating resin can be covered at the rear face of this semiconductor device, a track on the back can be dented, or wiring prepared in the rear face of a semiconductor device at the mounting substrate can be made to extend by making it project further. Therefore, multilayer structure is realizable with the track of a semiconductor device, a metal thin line, and wiring on a mounting substrate. Therefore, an electronic circuitry can be constituted, without adopting a multilayer substrate expensive as a mounting substrate. Moreover, in the former, although there is also a thing of 2 and 3 or 4 layer -- for which a multilayer substrate is adopted, the mounting substrate which reduced the number of layers is employable by adopting this semiconductor device.
[0150] Moreover, the thin shape and the lightweight circuit apparatus which consisted of necessary minimum of a semiconductor device, a track, and insulating resin are adopted, and since the track which said semiconductor device rear face moreover fixed is exposed from insulating resin, the track by the side of a mounting substrate and the hybrid integrated circuit equipment which can fix can be offered.
[0151] Therefore, the heat of a built-in circuit element can be made to radiate heat to a mounting substrate side, and, moreover, thin and more nearly lightweight hybrid integrated circuit equipment can be offered. Moreover, since the side face of a track is bow structure, even if the whole circuit apparatus generates heat, the omission of a track and curvature can be inhibited. And since it has the heat dissipation structure which was excellent as hybrid integrated circuit equipment, the own temperature rise of a circuit apparatus can be controlled and the omission of a track and curvature can be prevented further. Therefore, the dependability of the whole hybrid integrated circuit equipment with which the thin shape and the lightweight circuit apparatus were mounted can be raised.
[0152] Furthermore, if a metal substrate is adopted as a mounting substrate, generation of heat of the circuit apparatus mounted can be inhibited, and the hybrid integrated circuit equipment which can pass an actuation current more can be offered.

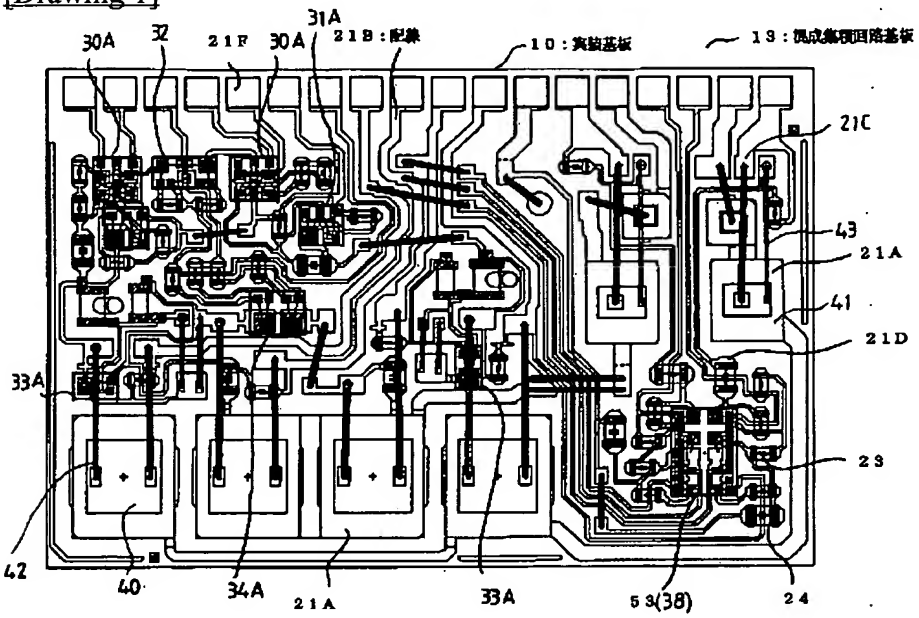
[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

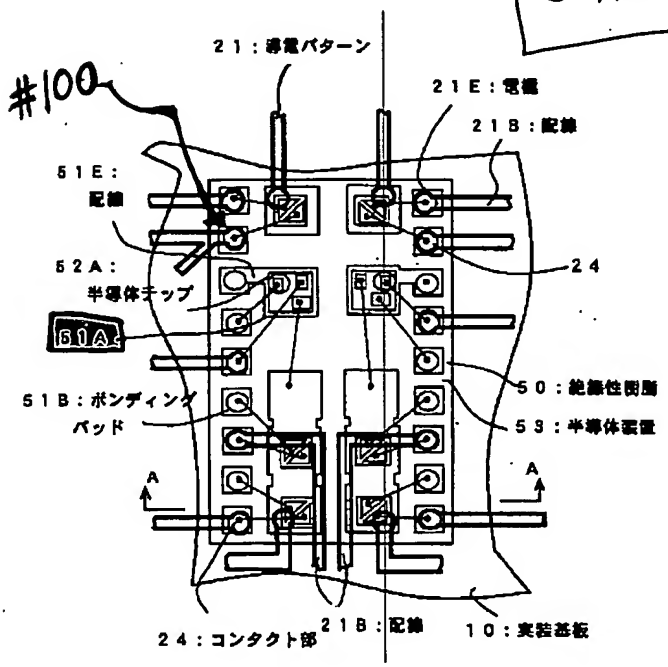
DRAWINGS

[Drawing 1]

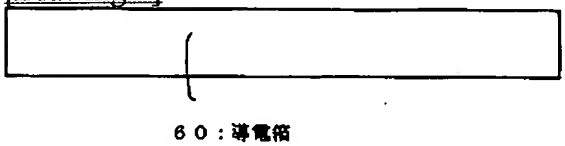


[Drawing 2]

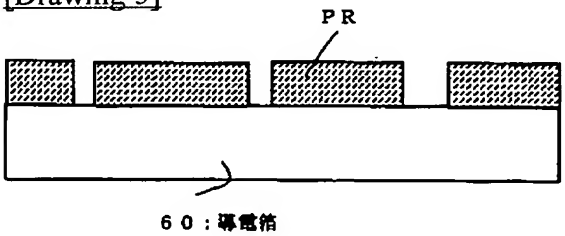
Drawing #2



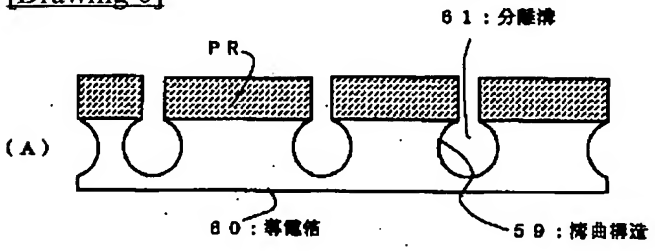
[Drawing 4]

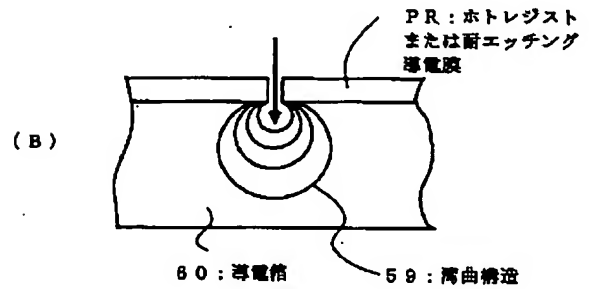


[Drawing 5]

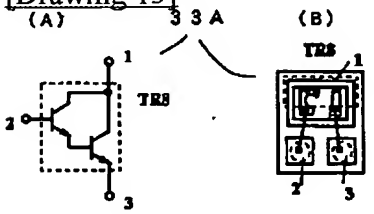


[Drawing 6]

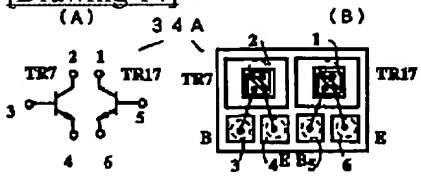




[Drawing 13]

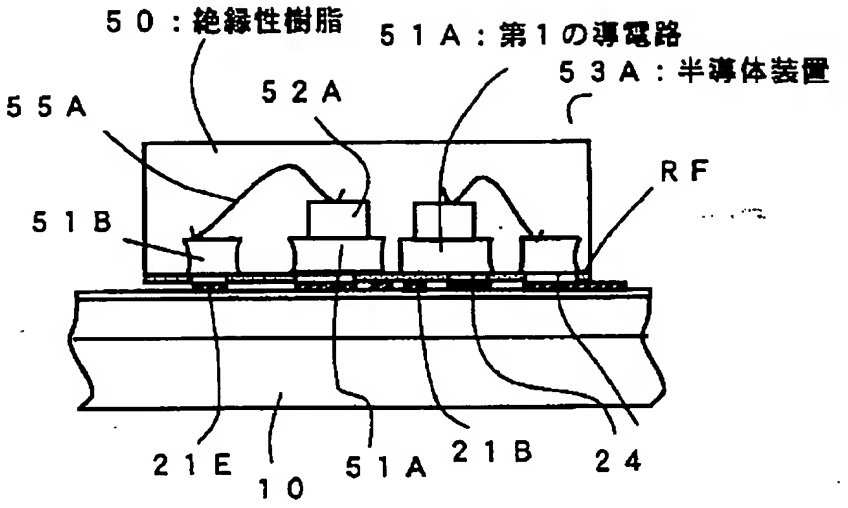


[Drawing 14]



[Drawing 3]

(A)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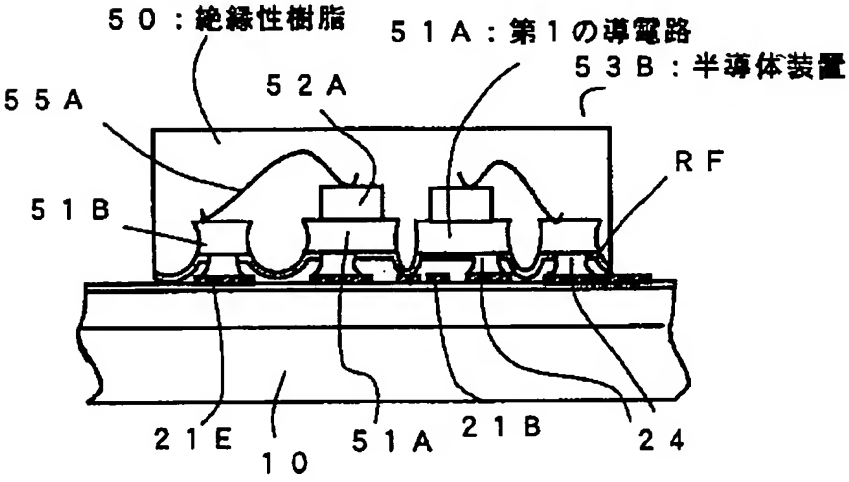
５１Ａ：第１の導電路
５３Ａ：半導体装置
５５Ａ
５２Ａ
ＲＦ
５１Ｂ
２１Ｅ
１０
５１Ａ
２１Ｂ
２４

(B)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５１Ａ：第１の導電路
５３Ｂ：半導体装置
５５Ａ
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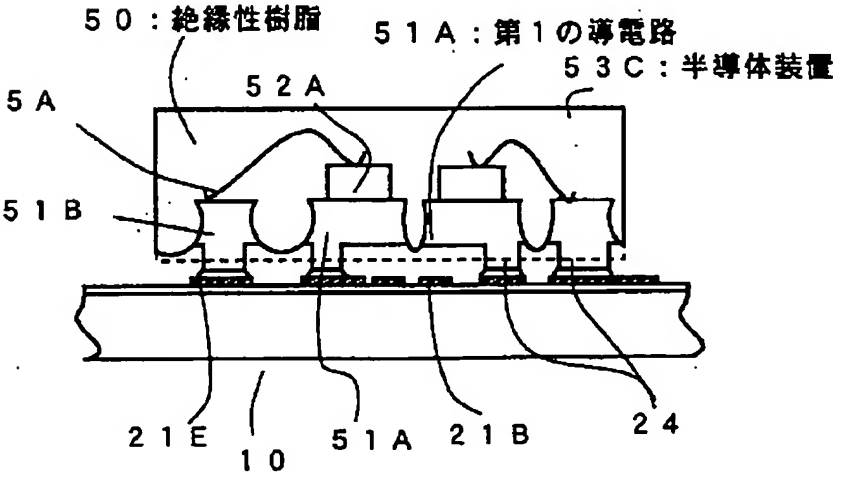
５１Ｂ
２１Ｅ
１０
５１Ａ
２１Ｂ
２４

(C)


５０：絶縁性樹脂
５１Ａ：第１の導電路
５３Ｃ：半導体装置
５５Ａ
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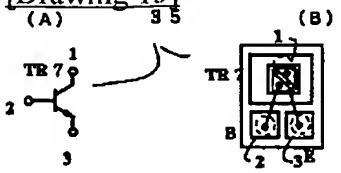
５１Ｂ
２１Ｅ
１０
５１Ａ
２１Ｂ
２４

[Drawing 15]



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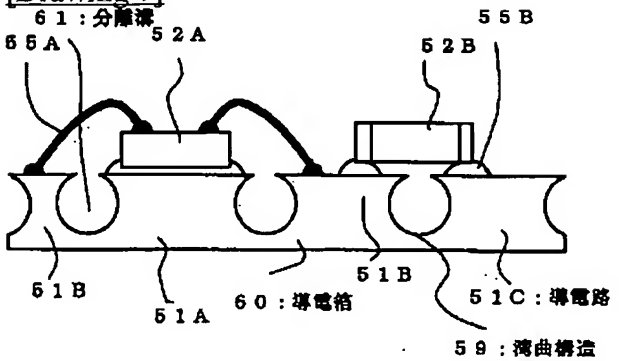
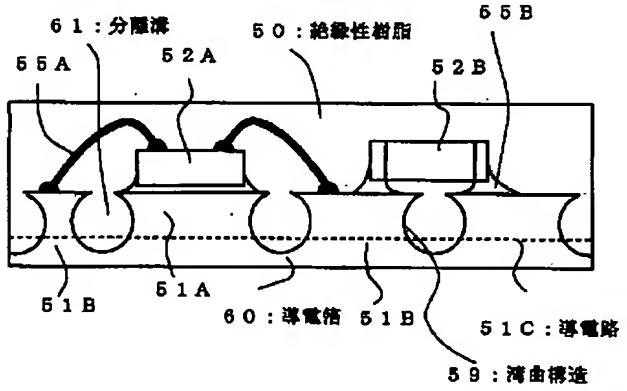
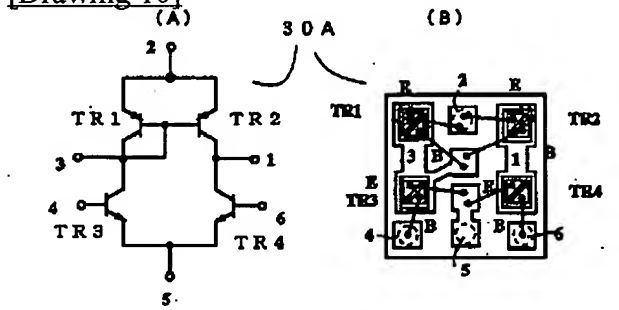


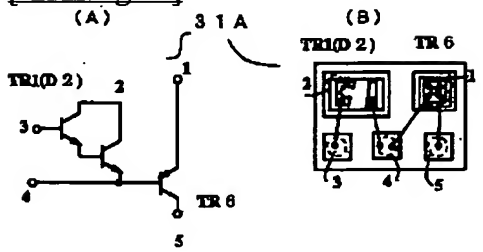
[Drawing 8]



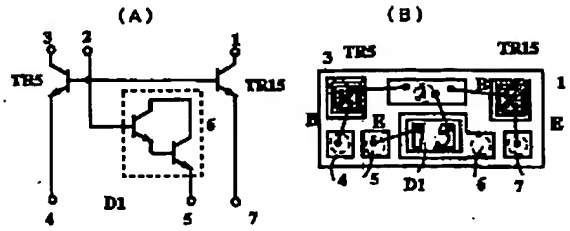
[Drawing 10]



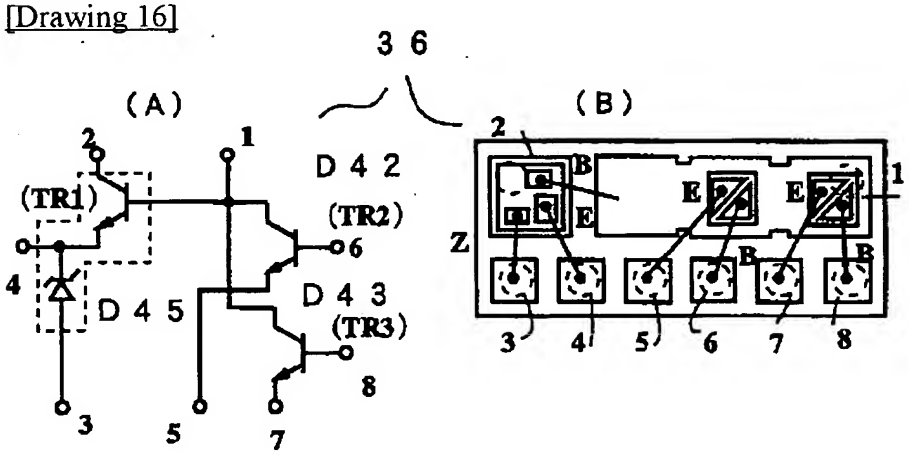
[Drawing 11]



[Drawing 12]

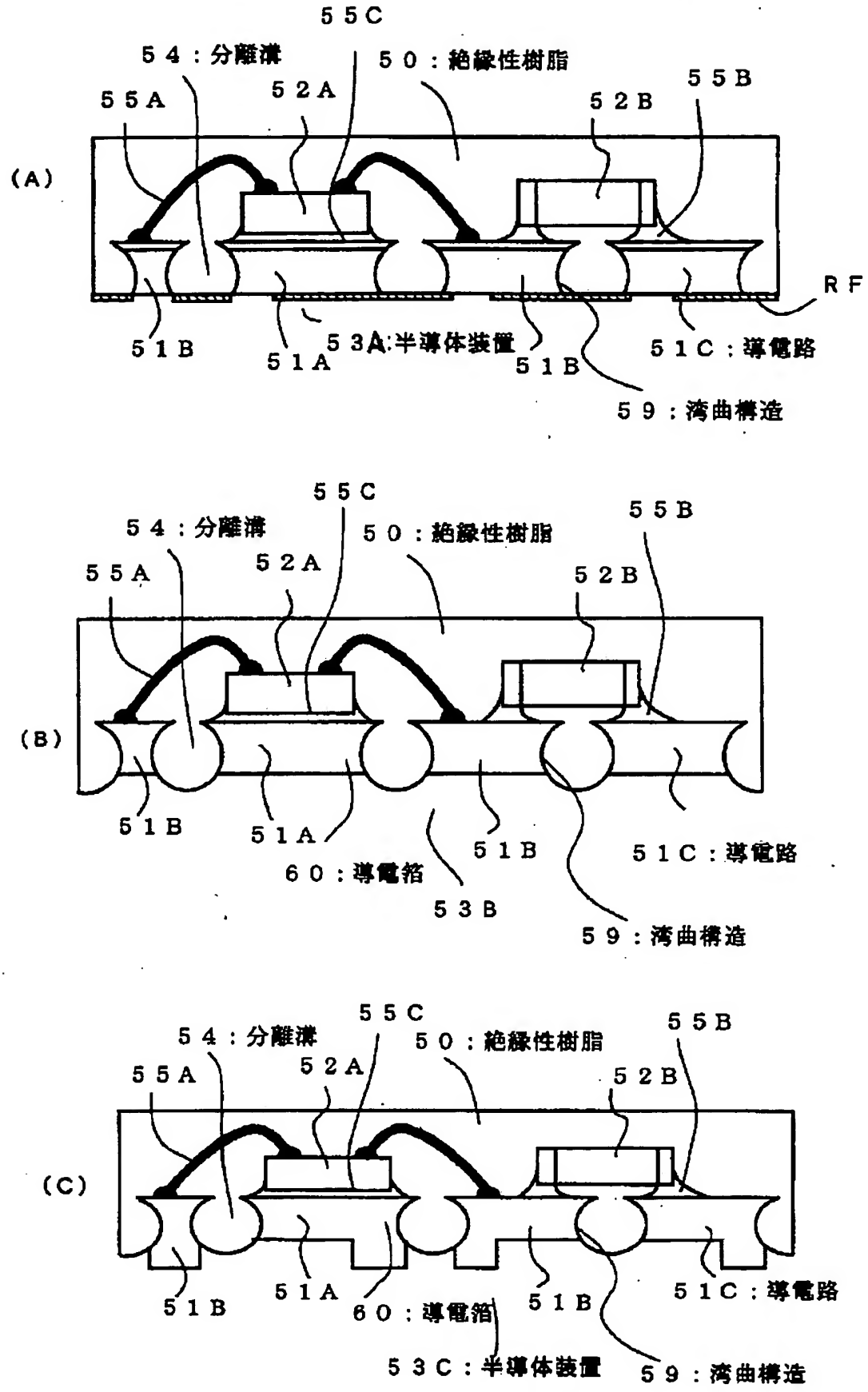


[Drawing 16]

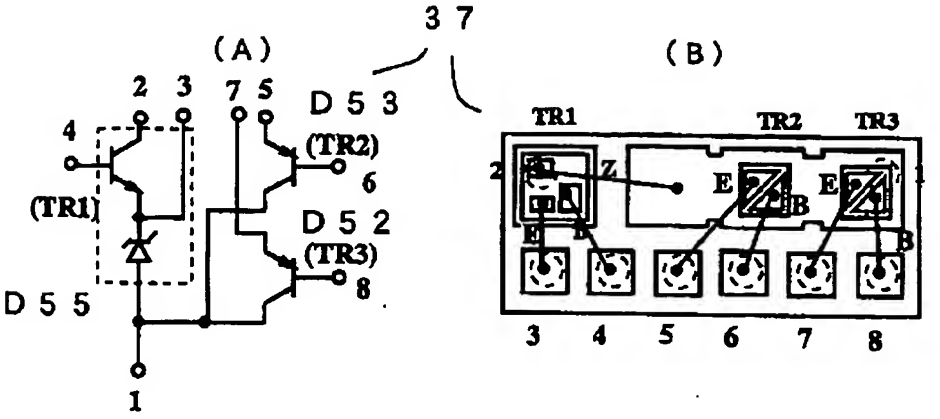


[Drawing 9]

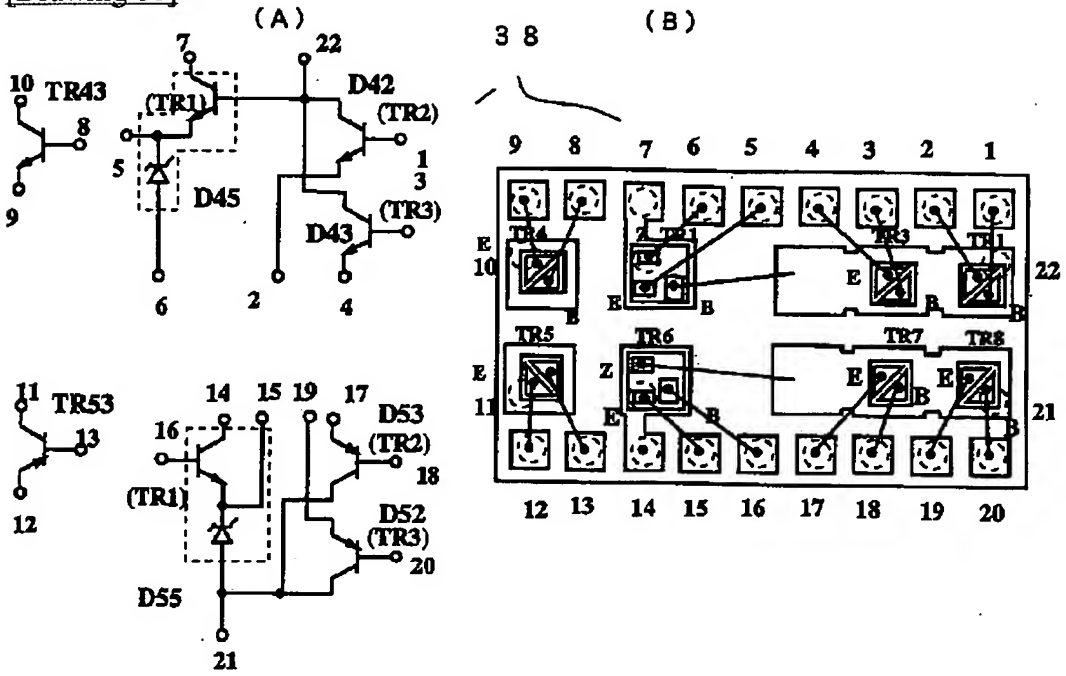
DRAWING #9



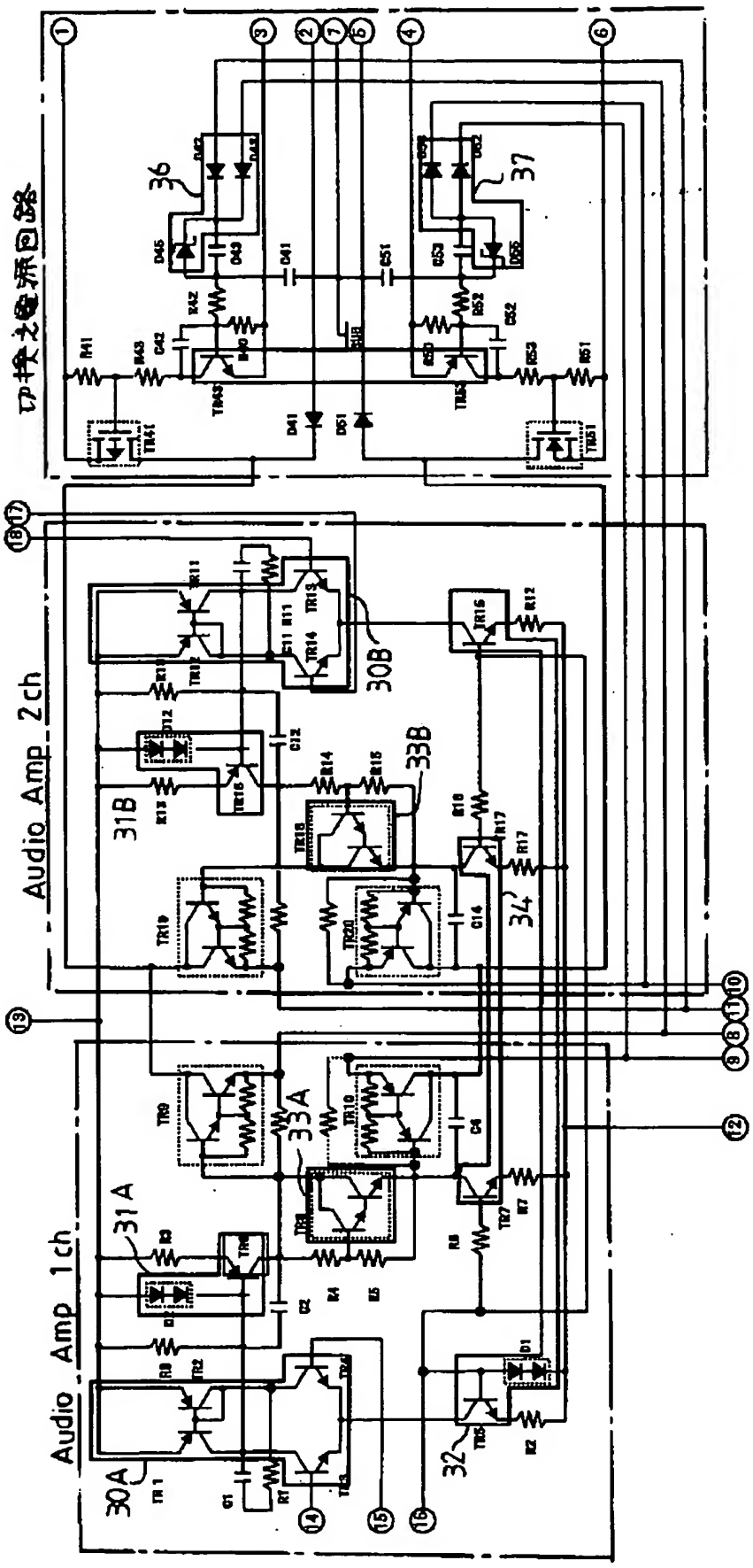
[Drawing 17]



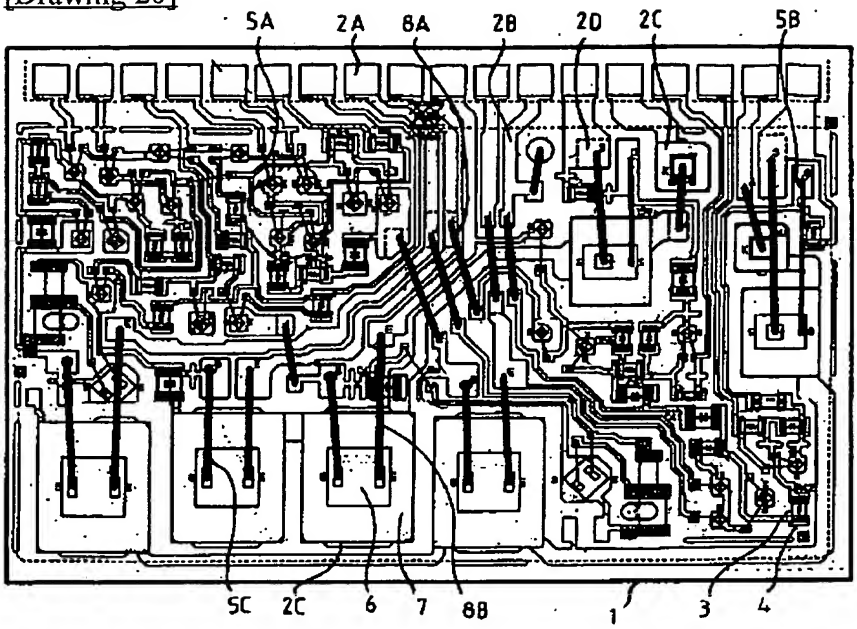
[Drawing 18]



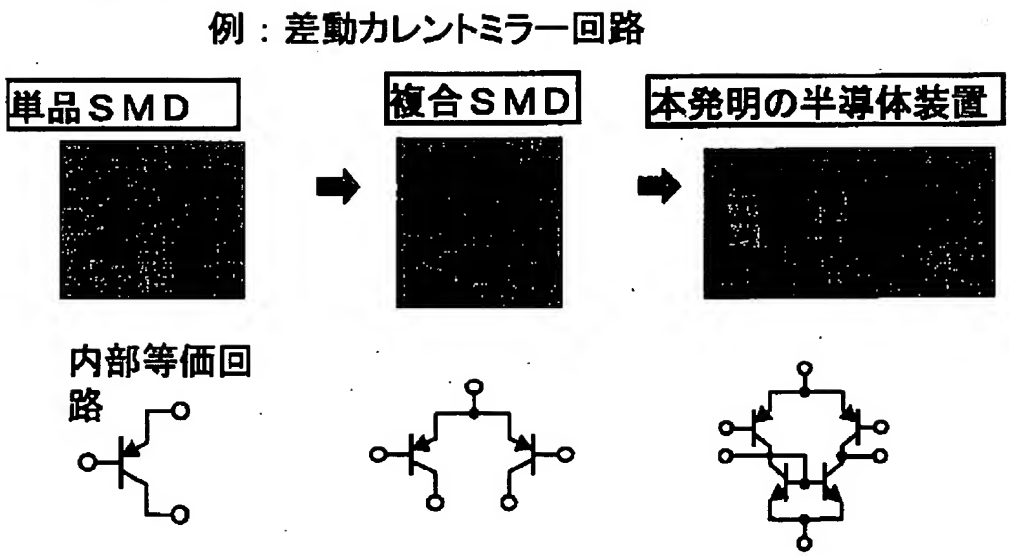
[Drawing 19]


Audio Amp 2ch
Audio Amp 1ch
30A
30B
31A
31B
32
33A
33B
34
36
37

[Drawing 20]



[Drawing 21]



[Translation done.]